photoresist.

[0041] These and other objects, features and advantages in the present invention will become apparent from the following brief description of the drawings, detailed description of the preferred embodiments, and appended claims and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] Fig. 1A illustrates the prior art step of sputter cleaning a semiconductor wafer;

[0043] Fig. 1B illustrates the prior art step of depositing an under bump metallurgy over a semiconductor wafer;

[0044] Fig. 1C illustrates the prior art steps of depositing, developing and patterning a photoresist layer to provide an opening over the contact pad on a semiconductor wafer;

[0045] Fig. 1D illustrates the prior art step of electroplating solder, and nickel and copper over the contact pad on a semiconductor wafer;

[0046] Fig. 1E illustrates a prior art step of removing the photoresist;

[0047] Fig. 1F illustrates a prior art step of removing the excess under bump metallurgy;

[0048] Fig. 1G illustrates the prior art step of reflowing the solder, copper, and nickel to form a bump on the semiconductor wafer;

[0049] Fig. 2A illustrates the step of a sputter cleaning a semiconductor wafer according to the present invention;

[0050] Fig. 2B illustrates the step of depositing an under bump metallurgy over a contact

pad on a semiconductor wafer according to the present invention;

[0051] Fig. 2C illustrates the steps of depositing a photoresist layer, developing and patterning the photoresist to form an opening down to the contact pad on the semiconductor wafer according to the present invention;

[0052] Fig. 2D illustrates the steps of electroplating a first electrically conductive material into the opening in the photoresist, and electroplating a second electrically conductive material on top of the first electrically conductive material according to the present invention;

[0053] Fig. 2E illustrates the step of removing the photoresist according to the present invention;

[0054] Fig. 2F illustrates a step of removing excess under bump metallurgy according to the present invention;

[0055] Fig. 2G illustrates the step of applying a flux agent over the second electrically conductive material according to the present invention;

[0056] Fig. 2H illustrates the step of hard baking the semiconductor device according to the present invention;

[0057] Fig. 2I illustrates the step of dipping a portion of the semiconductor wafer in an electroless plating solution according to the present invention;

[0058] Fig. 2J illustrates the step of removing the semiconductor wafer from the electroless plating solution to form a third electrically conductive material on top of the second electrically conductive material according to the present invention;

[0059] Fig. 2K illustrates a step of reflowing the electrically conductive materials to form a bump of improved height on the semiconductor wafer according to the present invention;

[0060] Fig. 3A illustrates an alternative embodiment of the invention wherein a flux agent is applied to the second electrically conductive material prior to removing the photoresist layer according to the present invention;

[0061] Fig. 3B illustrates the step of hard baking the semiconductor wafer according to the present invention;

[0062] Fig. 3C illustrates a step of removing the photoresist layer and excess under bump metallurgy according to the present invention;

[0063] Fig. 3D illustrates the step of dipping a portion of the semiconductor wafer in an electroless plating solution according to the present invention;

[0064] Fig. 3E illustrates the step of removing the semiconductor wafer from the electroless plating solution to provide a third electrically conductive material deposited on the second electrically conductive material according to the present invention; and

[0065] Fig. 3F illustrates a step of reflowing the electrically conductive materials to form a bump of improved height on the semiconductor wafer according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0066] Figs. 2A-K illustrate one embodiment of a method of making tall flip chip bumps according to the present invention. As shown in Fig. 2A, a semiconductor device 30 is provided